AN2353
Application note

Designing an application with the ST10F27x devices

Introduction

This note gives advice on designing applications based on devices of the ST10F27x family which includes the ST10F276, ST10F275, ST10F273, ST10F272 and ST10F271.

Six topics are covered:

- Information and recommendations on using an external resonator with the on-chip oscillator
- Details on start-up configuration and necessary precautions
- Filtering, decoupling and use of special pins
- Recommendations to reduce ADC conversion errors
- Memory interface
- Interfacing with the L4969 CAN interface

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1 Oscillator

The ST10F27x can run with an external clock connected to the XTAL1 input pin of the oscillator inverter or with a clock signal generated by a resonator connected to the XTAL1 / XTAL2 pins. According to the device, two kinds of oscillators have been implemented:

- ST10F276E, ST10F275E and ST10F273E: Wide-swing oscillator
- ST10F272E/B and ST10F271E/B: Low-power oscillator

Moreover, the ST10F27x provides a new feature when the Real Time Clock module is used and a reference clock is needed in Power Down mode. In this case, two possible configurations may be selected by the user application according to the desired level of power reduction:

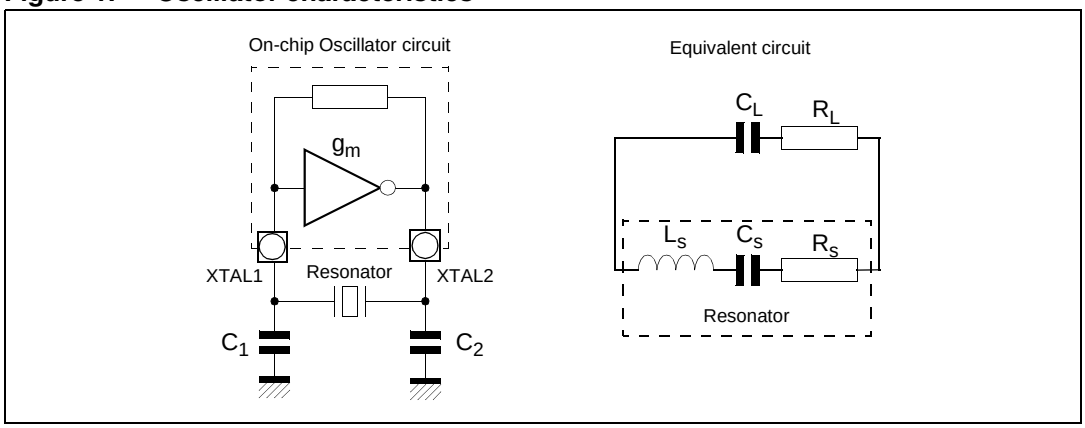
- A 32 kHz crystal is connected to the on-chip 32 kHz oscillator (pins XTAL3 / XTAL4) and running. In this case, the main oscillator is stopped when Power Down mode is entered, while the Real Time Clock continues counting using the 32 kHz clock signal as reference.
- Only the main oscillator is running (XTAL1 / XTAL2 pins). In this case, the main oscillator is not stopped when Power Down is entered and the Real Time Clock continues counting using the main oscillator clock signal as reference.

Refer to the ST10F27x datasheet for the possible combinations. This chapter provides detailed information on the use of the on-chip oscillator in conjunction with an external resonator.

1.1 Oscillator characteristics

Although simple to implement, using an external resonator (crystal or ceramic resonator) requires a few basic precautions. Referring to the schematic of the on-chip oscillator (*Figure 1*), the key items are described in the following section.

Figure 1. Oscillator characteristics



The resonator component can be a crystal or a ceramic resonator. It is represented as a series resonant branch R_S, L_S, C_S. The amplification ability of the oscillator inverter is replaced by a negative resistance R_L and the capacitance C_L contains the C_1 and C_2 load capacitances and the stray capacitance of the resonator.

The load capacitors C_1 and C_2 transform the gain of the amplifier (g_m) into a negative series resistance R_L to compensate for the losses of the crystal.

The best frequency stability is obtained when $C_1 = C_2$. The oscillation occurs when the sum of R_L and R_s (the series resistance of the crystal) is negative.

By choosing $C_1 = C_2 = C$, the minimal gain of the amplifier (g_m) is expressed as follows:

$$gm_{min} = Rs \times C^2 \times \omega^2 = Rs \times C^2 \times (2 \times \pi \times f)^2$$

The minimal gain of the amplifier also implicitly sets the on-chip oscillator start-up time.

Table 1. g_m values for different types of oscillators

Symbol	Parameter	Version	Conditions	Value			Unit
				Min	Typ	Max	
g_m	Oscillator transconductance	Wide-swing		8	17	35	mA/V
		Low-power		0.7	2.5	6	
		32 kHz	Start-up	20	31	50	µA/V
			Normal run	8	17	30	

The oscillation stability mainly depends on external parameters so only the transconductance (g_m) can be guaranteed and the start-up time value is defined by measurement at the application level.

1.2 Start-up time

Ceramic resonators have a much shorter start-up time than crystals (about 100 times faster) but have a lower accuracy on the frequency (initial tolerance, temperature variations and drift).

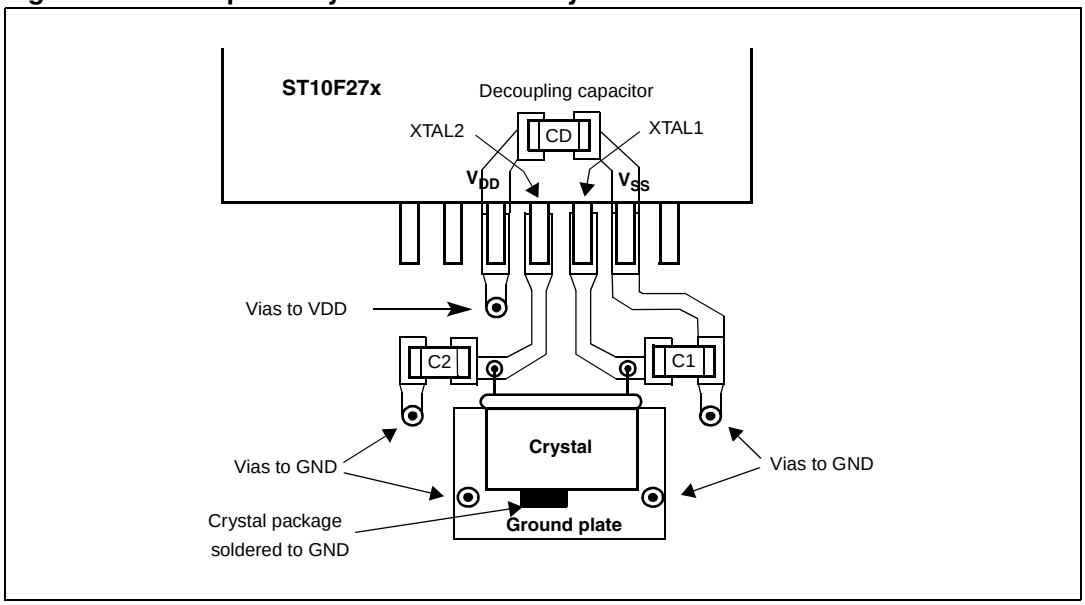
Depending on applications requirements and possibilities, users can choose between short oscillator start-up time and frequency accuracy.

From an ST10 perspective, the worst case condition / environment for the oscillator start-up time is high temperature and low voltage.

1.3 PCB layout for ST10F27x oscillator

The following *Figure 2* shows the proposed layout for the ST10F27x oscillator.

Figure 2. Example of layout for external crystal



1.4 Oscillator and EMC

The ST10F27x oscillator has an integrated gain control to minimize EMC and power consumption. However, this does not prevent users from observing / respecting the following rules / recommendations:

- Avoid other high frequency signals near the oscillator circuitry. These can influence the oscillator.
- Lay out/configure the ground supply on the basis of low impedance.
- Shield the crystal with an additional ground plane underneath the crystal.
- Do not lay out sensitive signals near the oscillator. Analyze cross-talk between different layers.
- The V_{SS} pin close to the XTAL pins must be connected to the ground plane and decoupled to the closest V_{DD} pin.
- Capacitors are placed at both ends of the crystal, directly connected to the ground plane while keeping the overall loop as small as possible.
- The crystal package, when metallic, is directly connected to the ground.

1.5 32 kHz oscillator

The same recommendations are valid for the 32 kHz oscillator. In any case, when the 32 kHz oscillator amplifier is not used, to avoid spurious consumption, XTAL3 must be tied to ground while XTAL4 is left open. Moreover, bit OFF32 in the RTCCON register should be set. The 32 kHz oscillator can only be driven by an external crystal and not by a different clock source.

2 Port0 start-up configuration

A reset sequence may be triggered for the following reasons:

- Hardware reset signal on pin $\overline{\text{RSTIN}}$ (hardware reset input)
- Execution of the software reset instruction SRST
- Overflow of the Watchdog Timer

After recognition of a reset, the ST10F27x proceeds with the actions listed below:

- Complete internal RAM write operation before the internal reset procedure begins
- Cancel pending internal hold states
- Abort external memory access cycles
- Start program execution from memory location 0000h in code segment 0

Note: Please refer to the datasheet and user's manual for reset event definitions.

2.1 Port0

Pull-down resistors

Pull-down resistors should be low enough so that the input voltage in P0.x is within the circuit specification when taking into account the circuit pull-up current (see PORT0 configuration current for $V_{in} = V_{ILmax}$) and other leakage currents from external circuits connected to PORT0 pins.

$$R_{pd} < (V_{ILmax}) / (I_{POl} + I_{other\ circuits})$$

Recommended maximum value: $R_{pd} = 8K\Omega$; commonly used values, although larger than the calculated result, are $10K\Omega$

Pull-up resistors

PORT0 supplies internal pull-up resistors that are active during Reset. Pull-up resistors should be low enough so that the input voltage in P0.x is within the circuit specification when taking into account the circuit pull-up current (see PORT0 configuration current for $V_{in} = V_{IHmin}$) and other leakage currents from external circuits connected to PORT0 pins. For worst case evaluation, leakage current from other external circuits should always be added to circuit leakage current.

$$R_{pu} < (V_{ddmin} - V_{IHmin}) / (I_{other\ circuits} - I_{POh})$$

No external pull-up resistor is necessary if $I_{other\ circuits} < I_{POH}$.

Table 2 presents the clock options on PORT0 P0H.5 - P0H.7 for devices with low power oscillator.

Table 3 presents the clock options on PORT0 P0H.5 - P0H.7 for devices with wide-swing oscillator.

Table 2. Clock options on PORT0 P0H.5/.7 for devices with low-power oscillator

P0H.7	P0H.6	P0H.5	CPU frequency $f_{CPU} = f_{XTAL}$ x F	External clock input range(1)	Notes
1	1	1	f_{XTAL} x 4	4 to 8 MHz	Default configuration
1	1	0	f_{XTAL} x 3	5.3 to 8 MHz	
1	0	1	f_{XTAL} x 8	4 to 8 MHz	
1	0	0	f_{XTAL} x 5	6.4 to 8 MHz	
0	1	1	f_{XTAL} x 1	1 to 64 MHz	Direct drive(2)
0	1	0	f_{XTAL} x 10	4 to 6.4 MHz	
0	0	1	f_{XTAL} x 0.5	4 to 8 MHz	CPU clock via prescaler(3)
0	0	0	f_{XTAL} x 16	4 MHz	

1. The external clock input range refers to a CPU clock range of 1...64 MHz.
2. The maximum input frequency depends on the duty cycle of the external clock signal (refer to the latest datasheet).
3. The limit on input frequency is 4 to 8 MHz since the usage of the internal oscillator amplifier is required. Also, when the PLL is not used and the CPU clock corresponds to FXTAL/2, an external crystal or resonator should be used: It is not possible to force any clock with an external clock source.

Table 3. Clock options on PORT0 P0H.5 /.7 for devices with wide-swing oscillator

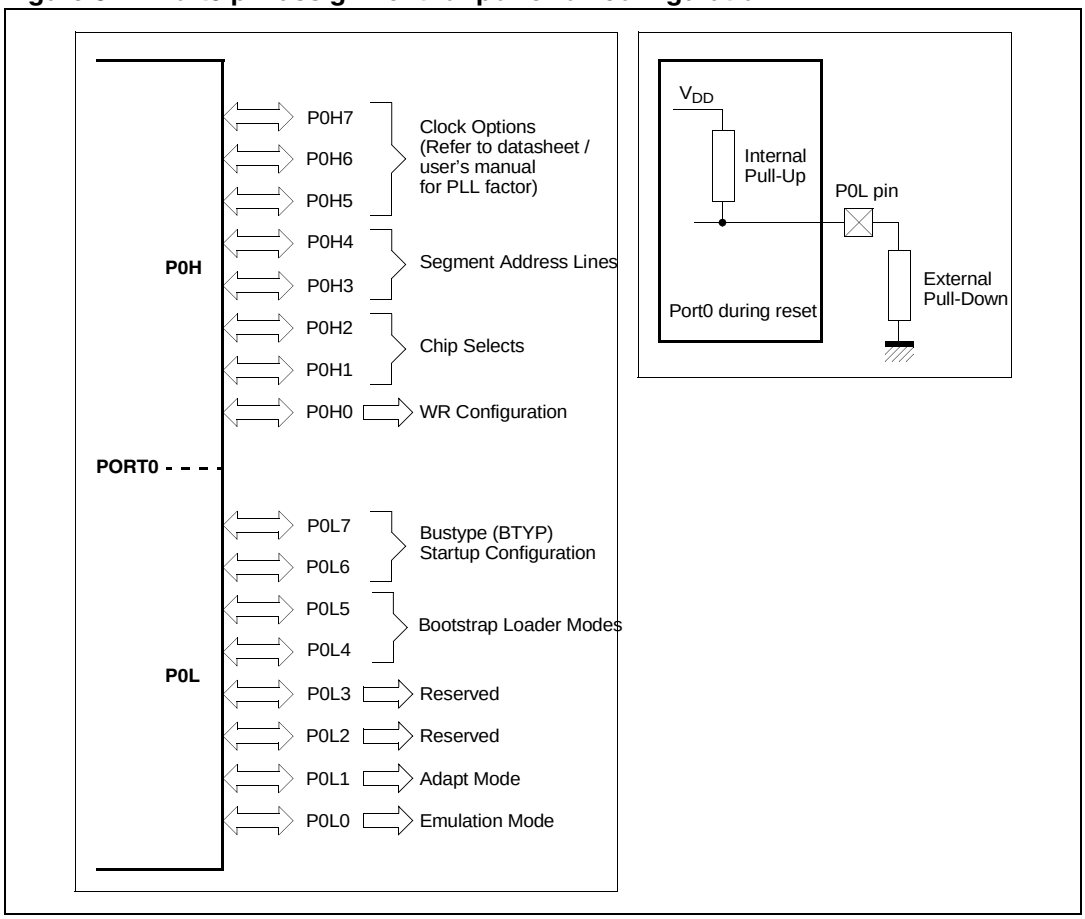
P0H.7	P0H.6	P0H.5	CPU frequency $f_{CPU} = f_{XTAL}$ x F	External clock input range(1)	Notes
1	1	1	f_{XTAL} x 4	4 to 8 MHz	Default configuration
1	1	0	f_{XTAL} x 3	5.3 to 10.6 MHz	
1	0	1	f_{XTAL} x 8	4 to 8 MHz	
1	0	0	f_{XTAL} x 5	6.4 to 12 MHz	
0	1	1	f_{XTAL} x 1	1 to 64 MHz	Direct drive(2)
0	1	0	f_{XTAL} x 10	4 to 6.4 MHz	
0	0	1	f_{XTAL} x 0.5	4 to 12 MHz	CPU clock via prescaler(3)
0	0	0	f_{XTAL} x 16	4 MHz	

1. The external clock input range refers to a CPU clock range of 1...64 MHz.
2. The maximum input frequency depends on the duty cycle of the external clock signal (refer to the latest datasheet).
3. The limit on input frequency is 4 to 12 MHz since the usage of the internal oscillator amplifier is required. Also when the PLL is not used and the CPU clock corresponds to FXTAL/2, an external crystal or resonator shall be should be used: It is not possible to force any clock withan external clock source.

2.2 Port0 start-up configuration

Figure 3 illustrates the usage of PORT0 pins to configure ST10F27x. All pins are sampled at power-on reset but some of them are not sampled for specific reset conditions. For details, please refer to the product datasheet and application note.

Figure 3. Port0 pin assignment for power-on configuration



3 Filtering / decoupling

3.1 Decoupling on V_{18} pins

V_{18} is the output of the ST10F27x internal voltage regulator. It is available on the package to connect external decoupling capacitors.

A capacitor, X7R dielectric or equivalent, with a minimum value of 10nF (and maximum 100nF) must be connected between this pin and its nearest V_{SS} pin. This is done to decouple the output of the internal regulator from the ground.

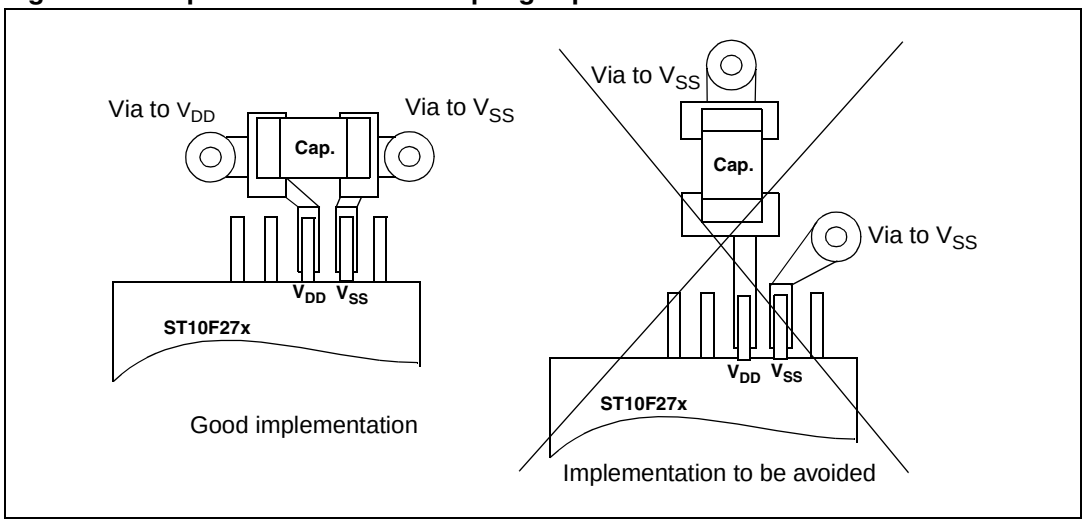
3.2 Decoupling on +5V supply

Decoupling capacitors are placed as close as possible to the chip V_{SS}/V_{DD} pins:

- Connected to both V_{DD} and V_{SS} pins (adjacent pins)
- Connected to each V_{DD}/V_{SS} pair

For EMC reasons, decoupling capacitors are connected to the V_{DD} and V_{SS} of adjacent pins. This is illustrated by *Figure 4* below:

Figure 4. Implementation of decoupling capacitors



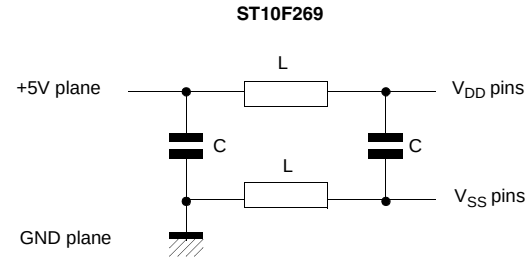
3.3 Filtering / EMC

As ST10F27x has an internal voltage regulator, +5V pins are not differentiated between output-buffers and internal logic. This means that when EMC filters are used to isolate the CPU from the supply, all ST10F27x supply pins should be isolated with the filter(s).

Example of filter

Filter placed on supply line of the CPU to remove the conducted noise from the supply line of the module (as illustrated in *Figure 5*).

Figure 5. Filter based on discrete components



Filter connected to supply line of the CPU

3.4 Unused general purpose pins

Unused pins may be an additional source of noise if not properly connected.

Used pins must **NOT** be left floating.

Two configurations are possible:

1. Unused pins configured as input (default after reset)

   Connect the unused pin to V_{SS} (directly or via a pull-down resistor)

2. Unused pin configured as output (by user software)

   The software sets the corresponding bit of the Direction Port Registers (DPPx) to configure an unused pin as an output (set direction bit to 1) with level to V_{SS} (data bit to 0, default after reset). In this condition, the pad can be left unconnected on the board.

Note: Avoiding floating pins in an application also ensures a good control on power consumption.

- Special handling for pins of Port 0 and Port 6

On the pins of Port 0 and Port 6, internal pull-ups are present (under Reset only). Our recommendation is: to keep them open and configured by software as output (set direction bit to 1) with output = 0 (data = 0).

- Special handling for pin P3.12 and $\overline{\text{BHE}}$ functionality

The pin P3.12 can be used as the $\overline{\text{BHE}}$ (Byte High Enable) signal for the external memory interface. The $\overline{\text{BHE}}$ alternate function is automatically enabled when the start-up configuration under Reset selects a 16-bit data bus.

There are two ways of disabling the $\overline{BHE}$ alternate function on P3.12:

– Select an 8-bit data bus size on Port0 during reset (pin P0L7 to V_{SS}).
– Disable it via bit BYTDIS of the SYSCON register.

4 Special pins

4.1 External access enable/stand-by voltage supply pin ($\overline{EA}/V_{STBY}$)

A low level applied to this pin during and after reset forces the ST10F27x to start the program execution from the external memory space. A high level will start the program execution from internal memory.

If only internal memory is used, this pin can be tied directly to V_{DD}.

The $\overline{EA}/V_{STBY}$ pin is also used (when Stand-by mode is entered, that is, ST10F27x under reset and main V_{DD} turned off) to bias the 32 kHz oscillator amplifier circuit, to provide a reference voltage for the low-power embedded voltage regulator which generates the internal 1.8V supply for the XRTC module (when not disabled) and to retain data inside the Stand-by portion of the XRAM (16 Kbyte). It can range from 4.5 to 5.5V.

4.2 RPD Pin

The RPD pin (Return from Power-Down) generates the proper internal timing sequence when interruptible power-down mode is used.

If the interruptible power-down mode is not used, the RPD pin can be connected to the ground (directly or via a resistor of 1M maximum). In this configuration, the device always performs asynchronous resets.

For more details, please refer to application note AN2340, *ST10 RPD pin: Functionality during Reset and Power-down mode.*

5 Reset

For information on ST10F27x reset, please refer to the product user manual.

6 Analog Digital Converter (ADC)

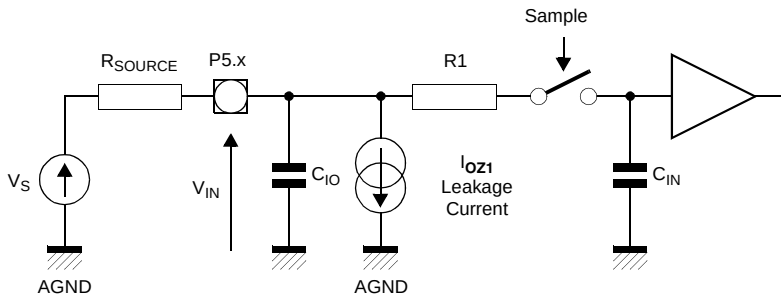
Analog input signal error can be created by poor matching of the source internal resistance with the ADC input parameters, which can be caused by the following occurences:

- Voltage drop in the voltage source resistance due to input leakage current
- Poor charging of the ADC internal capacitance (C_{in})

Analog input error can also be caused by noise from the analog input signal.

This section describes each of these causes.

Figure 6. Source internal resistance errors



I_{OZ1} (Input leakage current Port5): maximum ± 200nA (test condition: 0.45V < V_{IN} < V_{DD})
C_{IO} (Pin capacitance Port5): maximum 10pF (test condition: f = 1 MHz, T_A = 25°C, guaranteed by design characterization)
C_{IN} (ADC internal capacitance): maximum 5pF (guaranteed by design characterization)
R1 (Series input resistance): maximum 1.5kΩ (guaranteed by design characterization)

6.1 Voltage drop in the source resistance

The error generated by the voltage source internal resistance is:

$$error(LSB) = \frac{R_{SOURCE} \times I_{(0Z1)}}{V_{AREF} - V_{AGND}} \times 1024$$

$I_{(OZ1)}$ = specified leakage current.

Refer to the latest product datasheet for the value of $I_{(OZ1)}$.

Note: Input leakage current is caused by parasitic current into the on-chip protection of the input pin; this protection is necessary to protect the device against ESD (Electrical Static Discharge) and against overload.

6.2 Poor charging of the ADC internal resistance

During the sample time, the input capacitance (C_{IO} and C_{IN}) must be charged/discharged by the external source. The internal resistance of the source must allow the capacitance to reach its final value before the end of sample time.

If this does not happen, that is, if the source resistance is mismatched to the sample time, a voltage loss occurs at the sample and hold stage. This voltage loss causes an accuracy loss

when increasing or decreasing the input voltage from Varef/2 (hold capacitor is precharged to Varef/2 before sampling to reduce charge/discharge time).

Refer to the product data sheet for details.

6.3 Errors due to high frequencies from input signal

Small but high frequency signal variations can result in increased conversion error: During sampling time, the analog signal is fed to an internal auto-zero circuitry. Signal variations (at least two opposite transitions) during this time can generate auto-zero error. Signal variations during sampling time generate excessively high or low conversion results; big variations (Example: 150mV peak to peak variations at 1.5 MHz, with a 2.5V offset for 1µs sampling time) can generates clamped results (0x000 or 0x3FFh).

Although the sample and hold internal circuitry is integrating signal variations, other internal analog circuitry can be affected by signal transitions during sampling time.

The input analog signal should always be low pass filtered to ensure that high frequencies are rejected.

6.4 Reducing ADC errors

There are four possible optimizations:

- Minimize the total source impedance seen by the ST10

  This means choosing sensors with low output impedance (not always easy for some types of sensor) and minimizing the serial resistance of any protection devices between the analog source and the input pin (while still providing a voltage protection level compatible with the circuit specification).
- Match the sample time to the analog source impedance
- Match the sample time to the analog filter cut-off frequency to remove high frequencies

  The ST10F27x sampling time (ADC silicon configuration) shall be should be / must be / is 5 to 10 times shorter than the period of the cut-off frequency of the low-pass filter on ADC input signal.
- Reduce noise at the input pin

  Add an external RC filter (with attention to the source internal resistance). Compute the average value of different samples in the software routine.

6.5 Varef power-up and power-down sequence

Varef should always be lower than the 5V supply (maximum = V_{DD} + 0.1V). This is especially true for the power-up and power-down sequence when external devices are used to generate Varef.

7 External memory interface

The ST10F27x external memory bus can easily interface with the STMicroelectronics external Flash (M29Fxx series).

Please refer to application note AN1155 *Connecting the ST10 Microcontroller to M29 Series Flash Memories.*

8 Connecting to L4969

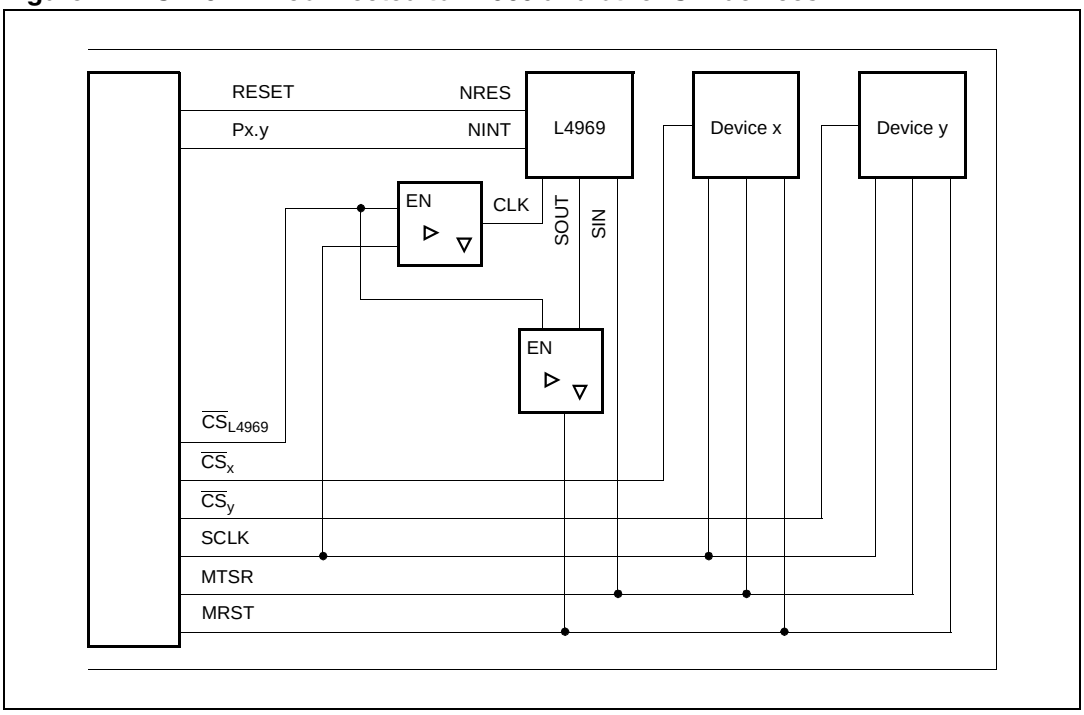
L4969 is a combined voltage regulator and low-speed CAN interface from STMicroelectronics.

The following figure shows how to connect the L4969 CAN interface to the ST10F27x microcontroller when working on an SPI bus with multiple peripherals.

Note: For further information on the L4969, please refer to the L4969 datasheet and the available application notes for this device.

When no other peripherals are connected to the SPI bus, the L4969 can be directly connected to the ST10 SPI lines without any further constraints.

Figure 7. ST10F27x connected to L4969 and other SPI devices



9 Revision history

Table 4. Document revision history

Date	Revision	Changes
24-Apr-2006	1	Initial release

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